

1 1. An integrated circuit comprising:

2 a plurality of data stream inputs and/or outputs that receive and/or transmit streams of
3 data;

4 a plurality of data stream processors that process the data streams, each data stream
5 processor being coupled to a data stream input and/or data stream output and including

6 a writeable instruction memory containing instructions; and

7 a receive processor that sequentially executes certain of the instructions to process the
8 data stream received from the data stream input and/or

9 a transmit processor that sequentially executes certain of the instructions to process the
10 data stream for output to the data stream output.

1 2. An integrated circuit comprising:

2 a plurality of data stream inputs and/or outputs that receive and/or transmit data streams;

3 a plurality of data stream processors that process the data streams, each data stream
4 processor being coupled to a data stream input and/or data stream output and including

5 a writeable local memory local to the data stream processor,

6 the plurality of local memories belonging to a global address space which is addressable by
7 any of the data stream processors.

1 3. An integrated circuit comprising:

2 a plurality of data stream inputs and/or outputs that receive and/or transmit data streams;

3 a plurality of data stream processors that process the data streams, each data stream
4 processor being coupled to a data stream input and/or data stream output; and

5 a context processor that responds to information received from a given data stream

6 processor that is processing a data stream to produce information about the given data stream's
7 context and provide the context information to the processor;

8 the given data stream processor using the context information to process the data stream.

1 4. The integrated circuit set forth in claim 3 wherein:

2 the context processor receives the information and provides the context information by
3 means of a bus on which there is an upper bound for latency for each of the data stream
4 processors and the context processor.

5. An integrated circuit comprising:

a plurality of data stream inputs and/or outputs that receive and/or transmit data streams, a data stream containing control data and a payload;

a plurality of data stream processors that process the data streams, each data stream processor being coupled to a data stream input and/or data stream output, a received data stream being processed to extract the control data and the payload and a transmitted data stream being processed to add control data to the payload;

a buffer manager that provides addresses of buffers for storing payload and responds to a write operation with a buffer address to write payload to the addressed buffer and to a read operation with a buffer address to read payload from the addressed buffer; and

a queue manager that manages queues of descriptors of payload, each descriptor including at least a buffer address, the queue manager responding to an enqueue command by enqueueing a descriptor provided with the command to a queue specified in the command and responding to a dequeue command by dequeueing a descriptor from the queue specified in the command,

a data stream processor responding to a received data stream by performing a write operation to the buffer manager with the received data stream's payload and an address provided by the buffer manager and performing an enqueue operation with a descriptor containing the address and transmitting a data stream by performing a dequeue operation, using the address in a descriptor obtained as a result of the dequeue operation in a read operation to the buffer manager, producing a data stream using the payload received from the buffer manager, and transmitting the produced data stream.

6. An integrated circuit comprising:

a plurality of data stream inputs and/or outputs that receive and/or transmit data streams;

a plurality of data stream processors that process the data streams, each data stream processor being coupled to a data stream input and/or data stream output; and

an aggregator that aggregates certain of the data stream processors so that the aggregated data stream processors cooperate in processing a data stream, the aggregator including

configurable interconnections between the aggregated data stream processors;

a configurable operation coordinator that coordinates operation of the aggregated data stream processors; and

11 a configurator that specifies the configurable interconnections and the configurable
12 operation coordinator as required to aggregate the data stream processors.

1 7. An integrated circuit comprising:

2 a plurality of data stream inputs and/or outputs that receive and/or transmit data
3 streams;

4 a plurality of data stream processors that process the data streams, each data stream
5 processor being coupled to a data stream input and/or data stream output and including

6 a control data processor,

7 a receive processor that processes data streams received from the data stream input
8 and/or

9 a transmit processor that processes data streams for output to the data stream output,
10 and

11 data structures that are shared by the control data processor, the receive processor
12 and/or the transmit processor and that contain information used by the receive processor and/or
13 the transmit processor and the control data processor to coordinate pipelined processing of a
14 data stream by the receive processor and/or the transmit processor and the control data
15 processor.

1 8. An integrated circuit comprising:

2 a plurality of data stream inputs and/or outputs that receive and/or transmit data
3 streams;

4 a plurality of data stream processors that process the data streams, each data stream
5 processor being coupled to a data stream input and/or data stream output and including

6 a receive processor that serially processes data streams received from the data stream
7 input and/or

8 a transmit processor that serially processes data streams for output to the data stream
9 output,

10 the receive processor and/or the transmit processor having a plurality of processing
11 components and being configurable to bypass one or more of the components in processing the
12 data streams.

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1 **9. An integrated circuit comprising:**

2 a plurality of serial data stream inputs and/or outputs that receive and/or transmit data
3 streams;

4 a plurality of data stream processors that process the data streams, each data stream
5 processor being coupled to a data stream input and/or data stream output and including

6 a receive processor that serially processes data streams received from the serial data
7 stream input and/or

8 a transmit processor that serially processes data streams for output to the serial data
9 stream output,

10 the receive processor writing a processed data stream to a memory and/or the transmit
11 processor reading a processed data stream from memory and the receive processor being
12 reconfigurable to read a data stream to be processed from the memory and/or the transmit
13 processor being reconfigurable to write a processed data stream to the memory.

1 **10. An integrated circuit comprising:**

2 a plurality of serial data stream inputs and/or outputs that serially receive and/or
3 transmit data streams;

4 at least one set of parallel data stream inputs and/or outputs that receive and/or transmit
5 data streams in parallel;

6 a plurality of serial data stream processors that process the data streams, each serial
7 data stream processor being coupled to a serial data stream input and/or data stream output and
8 including

9 a serial receive processor that processes data streams received from the serial data
10 stream input and/or

11 a serial transmit processor that processes data streams for output to the data stream
12 output; and

13 at least one parallel data stream processor that is coupled to the set of parallel data
14 stream inputs, each parallel data stream processor including

15 a parallel receive processor that processes data streams received from the set of parallel
16 data stream inputs, and/or

17 a parallel transmit processor that processes data streams for output to the set of parallel
18 data stream inputs.

1 **11.** An integrated circuit comprising:

2 a plurality of I/O pins that receive and/or transmit signals;

3 a data stream processor that processes data represented by the signals;

4 a writeable configuration specifier for specifying a configuration of a plurality thereof;

5 and

6 configuration circuitry coupled between the plurality of I/O pins and the data stream
7 processor and responsive to the configuration specifier for configuring the I/O pins as specified
8 by the configuration specifier,

9 whereby the integrated circuit may be used with a plurality of transmission protocols.

1 **12.** The integrated circuit set forth in claim 11 wherein:

2 the configuration specifier specifies electrical properties of the I/O pins; and

3 the configuration circuitry configures the I/O pins with the required electrical
4 properties.

1 **13.** The integrated circuit set forth in claim 11 wherein:

2 there is a plurality of data stream processors; and

3 the configuration specifier specifies which of the plurality of data stream processors are
4 connected to the plurality of I/O pins,

5 whereby a plurality of data stream processors may share processing of the data represented by
6 the signals received and/or transmitted by the plurality of I/O pins.

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